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Abstract
Vector quantization (VQ) has been widely used in communications and multimedia applications for signal compression due to its excellent rate-distortion performance. The method groups the source inputs into blocks (or vectors) and compares each input vector with each codevector in the codebook in order to find the codevector closest to the input vector. Then, the index corresponding to the closest codevector is transmitted to the decoder. The most popular codebook-search method is the full search algorithm (FSA). The FSA is simple but consumes longer time. Recently, many researchers address the triangle inequality elimination, the partial distance search, and the pyramid data structure to speed up searching and coding performance. This thesis proposed a fast search algorithm based on the particularly hierarchical technique to improve the speed of the VQ encoding process. The absolute value of sum difference is used to narrow search scope first. Next, a large number distance computation can be skipped by checking the absolute accumulated value of partial sums. Experiment results show that it achieves better search efficiency than other existed search algorithm. Besides, it can be easily implemented by hardware and applied to many real-time applications.

We also develop an efficient VLSI architecture to realize the proposed search algorithm. Using TSMC 0.35 Cell Library, the gate counts of the architecture is about 5722, and the chip size is 1819.6um*1818.6um. The maximum operating frequency is 55MHz. The hardware architecture is also implemented on an Altera FLEX10K FPGA chip. A demo system is built by integrating the chip with an 8051 microprocessor to verify the performance of our VLSI architecture.
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